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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,566	08/09/2001	Swee Yew Choe	P-6467	7266

7590

04/01/2002

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EXAMINER

CHANG, DANIEL D

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 04/01/2002 ✓

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

09/927,566

Applicant(s)

CHOE, SWEE YEW

Examiner

Daniel D. Chang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 1-4 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5-14 is/are allowed.
- 6) ☒ Claim(s) 15-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-4, drawn to a method for creating a cascaded chain of clocked half-rail differential logic circuits, classified in class 326, subclass 93.
- II. Claims 5-21, drawn to a method for creating a clocked half-rail differential logic circuit and a method for creating a cascaded chain using the clocked half-rail differential logic circuit, classified in class 326, subclass 95.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I and Group II are related as combination and subcombination.

Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the cascaded chain of Group I could use any of clocked half-rail differential logic devices. The subcombination has separate utility such as a particular clocked half-rail differential logic structure for use in variety of other circuits.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Philip McKay on March 21, 2002 a provisional election was made without traverse to prosecute the invention of Group II, claims 5-21.

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Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-4 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rovell (US 4,247,791) in view of Won et al (IEEE 0-7803-4455-3/98, "Modified Half Rail Differential Logic for Reduced Internal Logic Swing", pp. II-157 - II160).

Regarding claims 15-20, Rovell discloses, in fig. 2, a first supply voltage (Vdd), a second voltage (GND), a clocked differential circuit (10) having out terminal (14 or OUT), out-not terminal (16 or /OUT), second (PFET Q3), third (PFET Q4), fourth (PFET Q5), fifth transistors (NFET Q6), a logic block (NFETs Q1, Q2) with first (BIT) and second inputs (/BIT), and a clock signal (STROBE).

Rovell does not disclose a first transistor (a precharge transistor), with a clock-not signal coupled to the control electrode of the first transistor.

However, Won et al. disclose a precharge transistor with a clock-not signal coupled to the control electrode of the precharge transistor to exploit charge recycling technique and eliminate the necessity of high bias voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the differential circuit of Rovell with the precharge transistor as taught by Won et al. in order to lower power consumption.

Regarding claim 21, Rovell does not disclose that the fourth transistor is NFET.

However, it is well known in the art that an NFET provides much less space and greater speed and minimizes power dissipation compare to a PFET. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to substitute the PFET (Q5) of Rovell with the well known NFET in order to improve speed, space and power consumption.

Allowable Subject Matter

Claims 5-14 are allowable.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Revel, taken alone or in combination of other references, does not teach or fairly suggest a method for creating a cascaded chain of clocked half-rail differential logic circuits, as set forth in the claims.

Conclusion

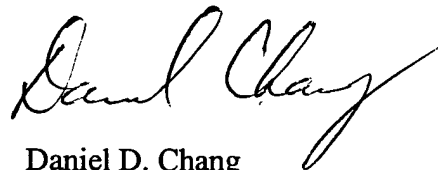
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A handwritten signature in black ink, appearing to read "Daniel Chang", written in a cursive style.

Daniel D. Chang
Examiner
Art Unit 2819

DC
March 21, 2002